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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/530,899
Filing Date: October 26, 2005
Appellant(s): DIEHL, ERIC

Daniel E. Sragow
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/14/2008 appealing from the Office action mailed 1/22/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: The Examiner has rejected Claim 1 – 3 and 6 – 8 under 35 USC 103 (a) as unpatentable over an article by Jouppi et al in view of US Patent 4,008,460 to Bryant et al.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Jouppi et al., "Tradeoffs in Two-Level On-Chip Caching"

1994, IEEE Computer Society Press, Pages 34 - 45

4,008,460	Bryant et al.	2-1977
5,513,336	Vishlitzky et al.	4-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 3 and 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi et al. "Tradeoffs in Two-Level On-Chip Caching" (herein after referred to as Jouppi) in view of Bryant et al. US Patent No. 4008460 (herein after referred to as Bryant).

Regarding claim 1, Jouppi describes a device for memorizing a list of items, said device being adapted to memorize an item presented thereto, said device being capable of memorizing N items (Two level exclusive caching, page 43, section 8) (Sizes of the cache levels are described, page 35, section 2.1), N being a natural integer, comprising: a first memory adapted to memorize a maximum of M items that were presented to said device (Desired lines are loaded directly to first level cache (page 43, section 8). Also Figure 8-1 (a) shows that the first level has a size of 4 lines for data), M being a natural integer less than N (size of first level cache being less than the total size of both first and second level cache (page 35, section 2.1)); a second memory adapted to memorize N-M second items, each of N-M items being different from each of said M items (Figure 8-1 (a) shows that the second level cache has a size of 16 lines for data. Under this scheme a mapping conflict in both first-level and second-level direct-mapped caches will give rise to "exclusion"; that is, the data involved in the mapping conflict will exist in one level of the hierarchy or the other, but not both (page 43, section 8). This is also shown in Figure 8-1 (a) since the item A in the first level cache is not present in the second level cache and there is no duplication of data), a victim of said M items in said first memory being moved to

said second memory (the first-level victim is sent to the second level cache (page 43, section 8)); means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device (Pseudo-random replacement (page 35, section 2.1)) (page 43, section 8); and means to memorize a first item in said device (page 43, section 8). Jouppi does not specifically describe that the first memory stores the M items that were last presented to said device, that an oldest of said M items in said first memory being moved to said second memory if said first memory already contains M items when a first item is presented for memorization or that the first item becomes a newest of said M items in said first memory.

Bryant describes that one replacement algorithm is LRU (least recently used), whereby the block in the buffer which was referenced least recently (i.e. longest not used) is assumed to be the least important, and therefore can be written over, i.e. replaced with minimum system performance impact (column 1, lines 13 – 18). It is further known that in an LRU replacement scheme that an item that has just been referenced becomes the most recently used. Items removed from would be the oldest items that have been least recently used.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a LRU replacement algorithm as described by Bryant with the first memory of Jouppi because LRU provides performance benefits by

replacing items which have been deemed to be least important because they have been least recently used (column 1, lines 13 – 18).

Regarding claim 2, Jouppi in view of Bryant describe the device according to claim 1 (see above), said device being adapted to supply information indicating whether said first item is already present in said device (cache hit (Jouppi, page 43, section 8 and page 37, section 2.5)).

Regarding claim 3, Jouppi in view of Bryant describe the device according to claim 1 (see above), said device being adapted to contain only one copy of each item memorized (Two-level exclusive caching (Jouppi, page 43, section 8). Also shown in Figure 8-1 (a), which represents an exclusive caching scheme, since item A is only present in the first level cache and not the second).

Regarding claim 6, Jouppi describes a method of memorizing an item in a device adapted to memorize an item presented thereto, said device being capable of memorizing N items (Two level exclusive caching, page 43, section 8) (Sizes of the cache levels are described, page 35, section 2.1), N being a natural integer, comprising: a first memory adapted to memorize a maximum of M items that were presented to said device (Desired lines are loaded directly to first level cache (page 43, section 8). Also Figure 8-1 (a) shows that the first level has a size of 4 lines for data), M being a natural integer less than N (size of first level cache being less than the total size of both first and second level cache (page 35, section 2.1)); a second memory adapted to memorize N-M second items, each of N-M items being different from each of said M items (Figure 8-1 (a)

shows that the second level cache has a size of 16 lines for data. Under this scheme a mapping conflict in both first-level and second-level direct-mapped caches will give rise to “exclusion”; that is, the data involved in the mapping conflict will exist in one level of the hierarchy or the other, but not both (page 43, section 8). This is also shown in Figure 8-1 (a) since the item A in the first level cache is not present in the second level cache and there is no duplication of data), a victim of said M items in said first memory being moved to said second memory (the first-level victim is sent to the second level cache (page 43, section 8)); means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device (Pseudo-random replacement (page 35, section 2.1)) (page 43, section 8); and means to memorize a first item in said device (page 43, section 8) said method describing: (a) receiving an item that is presented to the device (reference provided to determine cache hit/miss (Jouppi, page 43, section 8)); and (b) verifying whether said received item is already present in said device (Detecting cache hit/miss (Jouppi, page 43, section 8)); if said verification is negative, memorizing said received item in the device (Detecting cache hit/miss (Jouppi, page 43, section 8)). Jouppi does not specifically describe that the first memory stores the M items that were last presented to said device, that an oldest of said M items in said first memory being moved to said second memory if said first memory already contains M items when a first item is presented for

memorization, that the first item becomes a newest of said M items in said first memory or that if verification is positive that the received item is designated as an item last memorized in said device.

Bryant describes that one replacement algorithm is LRU (least recently used), whereby the block in the buffer which was referenced least recently (i.e. longest not used) is assumed to be the least important, and therefore can be written over, i.e. replaced with minimum system performance impact (column 1, lines 13 – 18). It is further known that in an LRU replacement scheme that an item that has just been referenced becomes the most recently used. Items removed from would be the oldest items that have been least recently used.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used a LRU replacement algorithm as described by Bryant with the first memory of Jouppi because LRU provides performance benefits by replacing items which have been deemed to be least important because they have been least recently used (column 1, lines 13 – 18).

Regarding claim 7, Jouppi in view of Byrant describe the method according to claim 6, further comprising if said verification in step (b) is negative: if said first memory does not already contain M items, memorizing said received item in said first memory (Jouppi, page 43, section 8); if said first memory already contains M items, transferring said oldest of said M items to said second memory (LRU of Bryant teaches that the oldest least recently used data should be removed since it is least important (column 1, lines 13 – 18)) (first-level victim of

Jouppi, page 43, section 8); and if said second memory already contains N-M items, randomly selecting one of said second items in said second memory for removal from said second memory, removing said randomly selected item, and memorizing said oldest of said M items in said second memory (pseudo random replacement of Jouppi, page 35, section 2.5).

Regarding claim 8, Jouppi in view of Bryant describe the device according to claim 2 (see above), wherein if said first item is already present in said device, said oldest item in said first memory is moved to said second memory and said first item is moved from said second memory to said first memory as said newest of said M items in said first memory (When a reference misses in the first level and hits in the second the contents of the first-level cache line are transferred to the second-level cache and the second-level cache is used to refill the first-level cache (Jouppi, page 43, section 8). LRU of Bryant would teach that the least recently used data would be removed from the first level and the new data coming from the second level would be the newest (most recently used)).

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi in view of Bryant as applied to claim 1 above, further in view of Vishlitzky et al. US Patent No. 5513336 (herein after referred to as Vishlitzky).

Regarding claims 4 and 5, Jouppi in view of Bryant describe the device according to claim 1 (see above). They do not specifically describe said device being adapted to memorize the number of times that said first item has been presented to said device or that said device being adapted to supply information

indicating whether said first item has already been presented to said device for a number of times that exceeds a predetermined number.

Vishlitzky describes the use of an access counter which is examined to determine how many times the data element has been accessed (column 16, lines 14 – 26). Examination of the access counter can determine if a data element has been accessed more than some number of times.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the access counter as described by Vishlitzky with the invention of Jouppi in view of Bryant because an access counter can determine the most or least recently used data in order to determine data that should be replaced upon a cache miss.

(10) Response to Argument

Appellant argues that it is clear that claims 1 and 6 require that the first and second memories contain no duplicated items. Furthermore, Appellant argues that since Jouppi specifically states that the arrangement provides for "less duplication between the contents of the first and second level cache" and that "Two-level exclusive caching reduces duplication of data between first level and second level caches, while providing additional associatively" that it is clear that Jouppi has duplication of information in their memories and therefore does not affect the patentability of claim 1.

Examiner explains that the presented argument fails to recognize that **no duplication is less duplication**. In two-level exclusive caching (each level

being a separate memory and therefore representing a first memory and second memory) data involved in the mapping conflict will exist in one level of the hierarchy or the other, **but not both** as shown in Figure 8-1 (a). Two-level exclusive caching provides no duplication (see Figure 8-1 (a)) which is less duplication that provided by two-level inclusive caching (as shown in Figure 8-1 (b)). Furthermore it would be advantageous to use two-level exclusive caching over two-level inclusive caching because the exclusive caching arrangement provides for more different items to be stored as exhibited by Figure 8-1 (a) since it holds A, B, C, D and E whereas Figure 8-1 (b) (inclusive) only holds A, A (duplicate), B, C and D.

Appellant argues that invention of Bryant et al. has duplication of data and therefore has no affect on the patentability of claims 1 and 6.

As explained in the rejection and response above, Jouppi is used to teach that there is no duplication of data in the memories (two-level exclusive caching) while Bryant was brought in to teach that the least recently used replacement algorithm is a conventional algorithm used to select a cache entry for replacement when the cache is full and a new entry needs to be stored.

Appellant argues that the combination of Jouppi and Bryant do not affect the patentability of claims 1 and 6 since neither of the cited references show or

suggest that each of the items in one memory is different from each of the items in another memory.

Examiner explains that the presented argument against Jouppi fails to recognize that **no duplication is less duplication**. In two-level exclusive caching (each level being a separate memory and therefore representing a first memory and second memory) data involved in the mapping conflict will exist in one level of the hierarchy or the other, **but not both** as shown in Figure 8-1 (a). Two-level exclusive caching provides no duplication (see Figure 8-1 (a)) which is less duplication that provided by two-level inclusive caching (as shown in Figure 8-1 (b)). Furthermore it would be advantageous to use two-level exclusive caching over two-level inclusive caching because the exclusive caching arrangement provides for more different items to be stored as exhibited by Figure 8-1 (a) since it holds A, B, C, D and E whereas Figure 8-1 (b) (inclusive) only holds A, A (duplicate), B, C and D. As explained above Bryant is used to teach that an LRU replacement technique is a well known and conventional replacement technique.

Appellant argues Examiner's reasoning that two-level exclusive caching has no duplication because of the previously presented statements made in Jouppi that supposedly indicate that there is duplication present.

Examiner explains that the presented argument fails to recognize that **no duplication is less duplication**. In two-level exclusive caching (each level

being a separate memory and therefore representing a first memory and second memory) data involved in the mapping conflict will exist in one level of the hierarchy or the other, **but not both** as shown in Figure 8-1 (a). Two-level exclusive caching provides no duplication (see Figure 8-1 (a)) which is less (reduced) duplication than what is provided by two-level inclusive caching (as shown in Figure 8-1 (a) exclusive caching, as compared to Figure 8-1 (b) which is inclusive caching). Furthermore it would be advantageous to use two-level exclusive caching over two-level inclusive caching because the exclusive caching arrangement provides for more different items to be stored as exhibited by Figure 8-1 (a) since it holds A, B, C, D and E whereas Figure 8-1 (b) (inclusive) only holds A, A (duplicate), B, C and D.

Appellant argues for claims 1 and 6 that Jouppi does not teach "means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device."

Examiner has cited that the invention of Jouppi uses **pseudo-random replacement** (page 35, section 2.1 and page 43, section 8). This **replaces** (removes) an item selected **randomly** when a new item must be stored and the memory is full.

Appellant argues that claims 2 – 5 and 8 are dependent from claim 1 and add further advantageous features. The Appellant submits that these sub claims are patentable as their parent claim 1.

Examiner refers to rejections and responses to arguments above as to why these claims are not allowable.

Appellant argues that claim 7 depends from claim 6 and adds further advantageous features. Appellant submits that claim 7 is patentable as its parent claim 6.

Examiner refers to rejections and responses to arguments above as to why these claims are not allowable.

Appellant argues that Vishlitzky does not teach "means for randomly selecting one of said second items memorized in the second memory and for removing the selected item if said second memory already contains N-M items when said first item is presented for memorization in said device."

Examiner has cited that the invention of Jouppi uses **pseudo-random replacement** (page 35, section 2.1 and page 43, section 8). This **replaces** (removes) an item selected **randomly** when a new item must be stored and the memory is full.

Appellant argues that Vishlitzky also does not teach "each of said N-M items being different from each of said M items."

Examiner explains that the presented argument fails to recognize that Jouppi teaches the presented limitation and that **no duplication is less duplication**.

In two-level exclusive caching (each level being a separate memory and therefore representing a first memory and second memory) data involved in the mapping conflict will exist in one level of the hierarchy or the other, **but not both** as shown in Figure 8-1 (a).

Two-level exclusive caching provides no duplication (see Figure 8-1 (a)) which is less duplication that provided by two-level inclusive caching (as shown in Figure 8-1 (b)).

Vishlitzky is used to teach the use of an access counter which is examined to determine how many times the data element has been accessed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ralph A Verderamo III/

Examiner, Art Unit 2186

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/Matt Kim/

Supervisory Patent Examiner, Art Unit 2186

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